

Low-Voltage, Dual Supply, Low r_{ON} , Quad SPST Analog Switches

FEATURES

- 2.7- thru 12-V Single Supply or ± 3 - thru ± 6 -Dual Supply
- On-Resistance— $r_{DS(on)}$: 1.7 Ω
- Fast Switching— t_{ON} : 42 ns
— t_{OFF} : 28 ns
- TTL, CMOS Compatible
- Low Leakage: 0.2 nA
- 2000-V ESD Protection

BENEFITS

- Widest Dynamic Range
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Simple Interfacing

APPLICATIONS

- Automatic Test Equipment
- Data Acquisition Systems
- Communication Systems
- ADC Systems
- xDSL and PBX/PABX
- Audio Signal Routing

DESCRIPTION

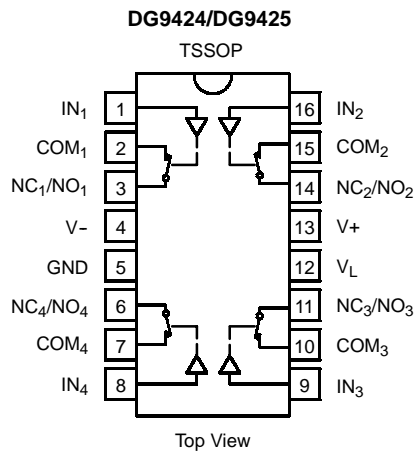
The DG9424/9425/9426 are low voltage precision monolithic quad single-pole-single-throw analog switches.

Using BiCMOS wafer fabrication technology allows the DG9424/9425/9426 to operate on single and dual supplies. Single supply voltage ranges from 3 to 12 V while dual supply operation is recommended with ± 3 to ± 6 V.

Combining high speed (t_{ON} : 42 ns), flat $r_{DS(on)}$ over the analog signal range (Ω), minimal insertion lose (-3 dB at 190 MHz), and excellent crosstalk and off-isolation performance, the DG9424/9425/9426 are ideally suited for audio and video signal switching.

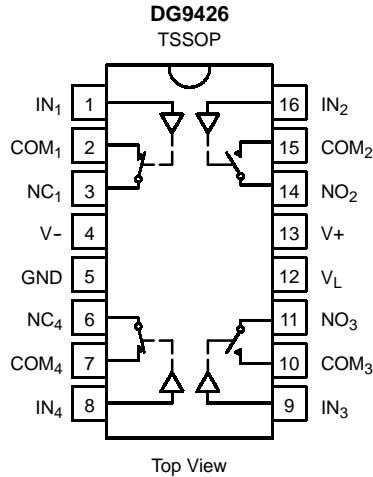
The DG9424 and DG9425 respond to opposite control logic as shown in the Truth Table. The DG9426 has two normally open and two normally closed switches.

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE		
Logic	DG9424	DG9425
0	OFF	ON
1	ON	OFF

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



TRUTH TABLE		
Logic	SW ₁ , SW ₄	SW ₂ , SW ₃
0	ON	OFF
1	OFF	ON

ORDERING INFORMATION		
Temp Range	Package	Part Number
DG9424/9425		
-40 to 85°C	16-Pin TSSOP	DG9424DQ
		DG9425DQ
DG9426		
-40 to 85°C	16-Pin TSSOP	DG9426DQ

ABSOLUTE MAXIMUM RATINGS

V+ to V- -0.3 TO 13 V
 GND to V- 7 V
 V_L (GND -0.3 V) to (V+) +0.3 V
 IN, COM, NC, NO^a -0.3 to (V+ +0.3 V)
 Continuous Current (NO, NC, COM Pins) 100 mA
 Peak Current, S or D (Pulsed 1 ms, 10% Duty Cycle) 200 mA
 Storage Temperature -65 to 150°C

Power Dissipation (Package)^b
 16-Pin TSSOP^c 450 mW

- Notes:
- a. Signals on NC, NO, COM or IN exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
 - b. All leads welded or soldered to PC Board.
 - c. Derate 5.6 mW/°C above 70°C



SPECIFICATIONS ^a (SINGLE SUPPLY 12 V)							
Parameter	Symbol	Test Conditions Unless Specified $V_+ = 12\text{ V}, V_- = 0\text{ V}$ $V_L = 5\text{ V}, V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp ^b	Limits -40 to 85°C			Unit
				Min ^d	Typ ^c	Max ^d	
Analog Switch							
Analog Signal Range ^e	V_{ANALOG}		Full	0		12	V
On-Resistance	r_{ON}	$V_+ = 10.8\text{ V}, V_- = 0\text{ V}$ $I_{NO}, I_{NC} = 50\text{ mA}, V_{COM} = 2/9\text{ V}$	Room Full		1.8	3 4	Ω
Digital Control							
Input Current	I_{INL} or I_{INH}		Full	-1	0.01	1	μA
Dynamic Characteristics							
Turn-On Time ^e	t_{ON}	$R_L = 300\ \Omega, C_L = 35\text{ pF}$ $V_{NO}, V_{NC} = 5\text{ V}$ See Figure 2	Room Full		42	57 65	ns
Turn-Off Time ^e	t_{OFF}		Room Full		28	42 44	
Break-Before-Make Time Delay ^e	t_D	DG9426 Only, $V_{NO}, V_{NC} = 5\text{ V}$ $R_L = 300\ \Omega, C_L = 35\text{ pF}$	Room	2			
Charge Injection ^e	Q_{INJ}	$V_g = 0\text{ V}, R_g = 0\ \Omega, C_L = 1\text{ nF}$	Room		38		pC
Off Isolation ^e	OIRR	$R_L = 50\ \Omega, C_L = 5\text{ pF},$ $f = 1\text{ MHz}$	Room		-56		dB
Channel-to-Channel Crosstalk ^e	X_{TALK}		Room		-77		
NO, NC Off Capacitance ^e	$C_{NO(off)}$ $C_{NC(off)}$	$f = 1\text{ MHz}$	Room		49		pF
COM Off Capacitance ^e	$C_{COM(off)}$		Room		37		
Channel On Capacitance ^e	$C_{COM(on)}$		Room		89		
Power Supplies							
Positive Supply Current	I_+	$V_{IN} = 0\text{ or }V_L$	Room Full		0.02	1 5	μA
Negative Supply Current	I_-		Room Full	-1 -5	-0.002		
Logic Supply Current	I_L		Room Full		0.002	1 5	
Ground Current	I_{GND}		Room Full	-1 -5	-0.002		

SPECIFICATIONS ^a (DUAL SUPPLY $\pm 5\text{ V}$)							
Parameter	Symbol	Test Conditions Unless Specified $V_+ = 5\text{ V}, V_- = -5\text{ V}$ $V_L = 5\text{ V}, V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp ^b	Limits -40 to 85°C			Unit
				Min ^d	Typ ^c	Max ^d	
Analog Switch							
Analog Signal Range ^e	V_{ANALOG}		Full	-5		5	V
On-Resistance	r_{ON}	$V_+ = 4.5\text{ V}, V_- = -4.5\text{ V}$ $I_{NO}, I_{NC} = 50\text{ mA}, V_{COM} = \pm 3.5\text{ V}$	Room Full		2	3.3 4.3	Ω
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	$V_+ = 5.5\text{ V}, V_- = -5.5\text{ V}$ $V_{COM} = \pm 4.5\text{ V}, V_{NO}, V_{NC} = \mp 4.5\text{ V}$	Room Full	-1 -10		1 10	nA
	$I_{COM(off)}$		Room Full	-1 -10		1 10	
Channel On Leakage Current	$I_{COM(on)}$	$V_+ = 5.5\text{ V}, V_- = -5.5\text{ V}$ $V_{NO}, V_{NC} = V_{COM} = \pm 4.5\text{ V}$	Room Full	-1 -10		1 10	
Digital Control							
Input Current ^a	I_{INL} or I_{INH}		Full	-1	0.05	1	μA



SPECIFICATIONS ^a (DUAL SUPPLY ± 5 V)							
Parameter	Symbol	Test Conditions Unless Specified $V_+ = 5\text{ V}, V_- = -5\text{ V}$ $V_L = 5\text{ V}, V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp ^b	Limits -40 to 85°C			Unit
				Min ^d	Typ ^c	Max ^d	
Dynamic Characteristics							
Turn-On Time ^e	t_{ON}	$R_L = 300\ \Omega, C_L = 35\text{ pF}$ $V_{NO}, V_{NC} = \pm 3.5\text{ V}$ See Figure 2	Room Full		56	74 81	ns
Turn-Off Time ^e	t_{OFF}		Room Full		42	64 67	
Break-Before-Make Time Delay ^e	t_D	DG9426 Only, $V_{NO}, V_{NC} = 3.5\text{ V}$ $R_L = 300\ \Omega, C_L = 35\text{ pF}$	Room	2			
Charge Injection ^e	Q_{INJ}	$V_g = 0\text{ V}, R_g = 0\ \Omega, C_L = 1\text{ nF}$	Room		112		pC
Off Isolation ^e	OIRR	$R_L = 50\ \Omega, C_L = 5\text{ pF},$ $f = 1\text{ MHz}$	Room		-56		dB
Channel-to-Channel Crosstalk ^e	X_{TALK}		Room		-82		
Source Off Capacitance ^e	$C_{NO(off)}$ $C_{NC(off)}$	$f = 1\text{ MHz}$	Room		38		pF
Drain Off Capacitance ^e	$C_{COM(off)}$		Room		38		
Channel On Capacitance ^e	$C_{COM(on)}$		Room		89		
Power Supplies							
Positive Supply Current ^e	I_+	$V_{IN} = 0\text{ or }V_L$	Room Full		0.03	1 5	μA
Negative Supply Current ^e	I_-		Room Full	-1 -5	-0.002		
Logic Supply Current ^e	I_L		Room Full		0.002	1 5	
Ground Current ^e	I_{GND}		Room Full	-1 -5	-0.002		

SPECIFICATIONS ^a (SINGLE SUPPLY 5 V)							
Parameter	Symbol	Test Conditions Unless Specified $V_+ = 5\text{ V}, V_- = 0\text{ V}$ $V_L = 5\text{ V}, V_{IN} = 2.4\text{ V}, 0.8\text{ V}^f$	Temp ^b	Limits -40 to 85°C			Unit
				Min ^d	Typ ^c	Max ^d	
Analog Switch							
Analog Signal Range ^e	V_{ANALOG}		Full			5	V
On-Resistance ^e	r_{ON}	$V_+ = 4.5\text{ V}, I_{NO}, I_{NC} = 50\text{ mA}$ $V_{COM} = 1\text{ V}, 3.5\text{ V}$	Room Full		3.4	4.8 5.8	Ω
Dynamic Characteristics							
Turn-On Time ^e	t_{ON}	$R_L = 300\ \Omega, C_L = 35\text{ pF}$ $V_{NO}, V_{NC} = 3.5\text{ V}$, See Figure 2	Room Hot		71	86 106	ns
Turn-Off Time ^e	t_{OFF}		Room Hot		37	51 56	
Break-Before-Make Time Delay ^e	t_D	DG9426 Only, $V_{NO}, V_{NC} = 3.5\text{ V}$ $R_L = 300\ \Omega, C_L = 35\text{ pF}$	Room	5			
Charge Injection ^e	Q_{INJ}	$V_g = 0\text{ V}, R_g = 0\ \Omega, C_L = 1\text{ nF}$	Room		10		pC
Power Supplies							
Positive Supply Current ^e	I_+	$V_{IN} = 0\text{ or }V_L$	Room Hot		0.02	1 5	μA
Negative Supply Current ^e	I_-		Room Hot	-1 -5	-0.002		
Logic Supply Current ^e	I_L		Room Hot		0.002	1 5	
Ground Current ^e	I_{GND}		Room Hot	-1 -5	-0.002		



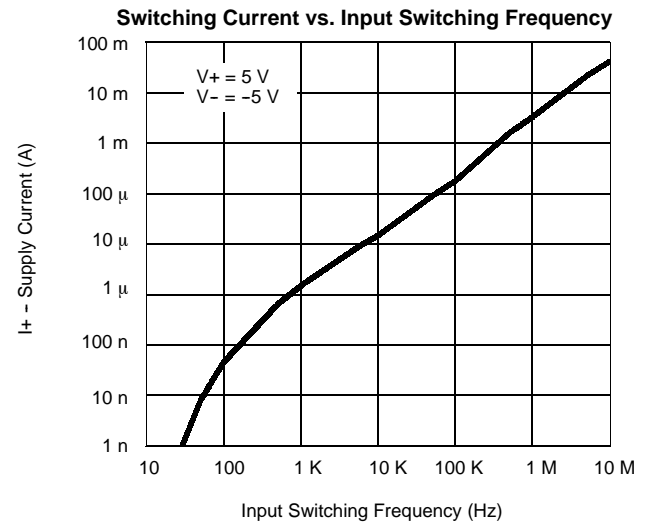
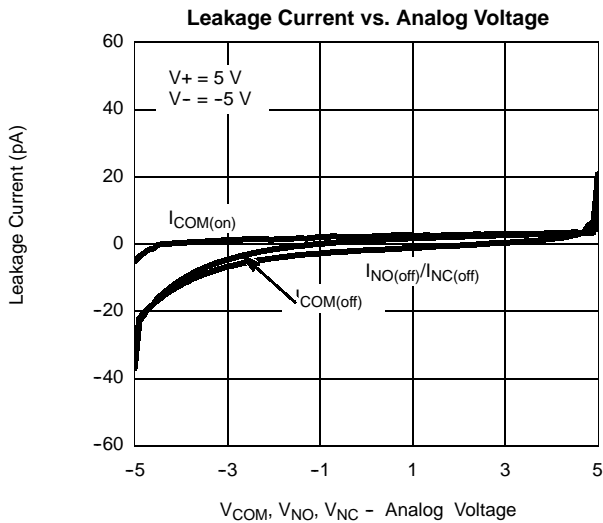
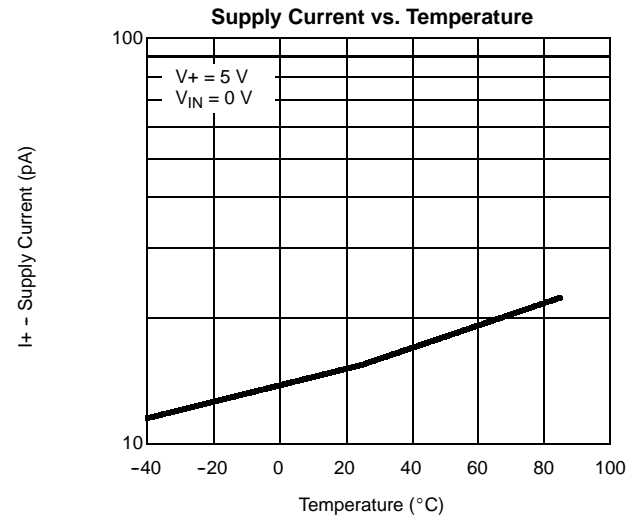
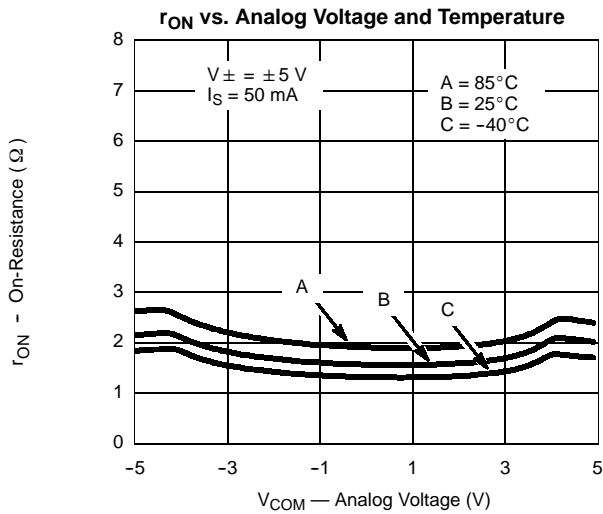
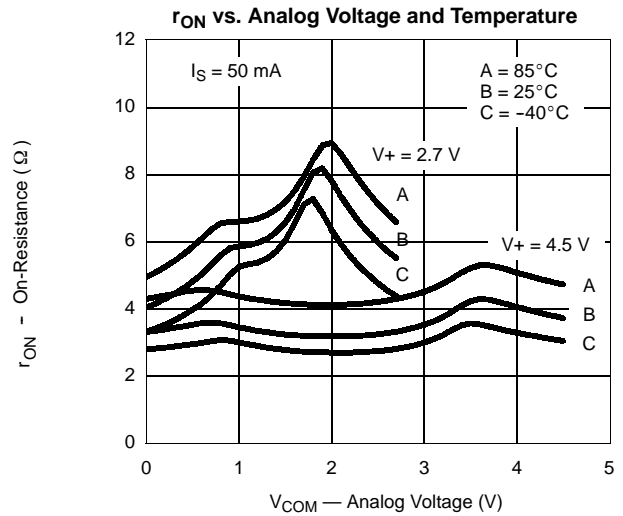
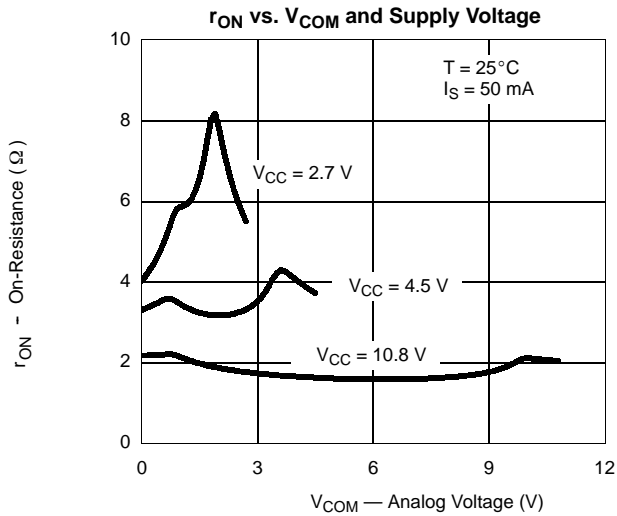
SPECIFICATIONS ^a (SINGLE SUPPLY 3 V)							
Parameter	Symbol	Test Conditions Unless Specified V ₊ = 3 V, V ₋ = 0 V V _L = 3 V, V _{IN} = 2.4 V, 0.4 V ^f	Temp ^b	Limits -40 to 85°C			Unit
				Min ^d	Typ ^c	Max ^d	
Analog Switch							
Analog Signal Range ^e	V _{ANALOG}		Full	0		3	V
On-Resistance	r _{ON}	V ₊ = 2.7 V, V ₋ = 0 V I _{NO} , I _{NC} = 5 mA, V _{COM} = 0.5, 2.2 V	Room Full		8	13.8 15.1	Ω
Switch Off Leakage Current ^a	I _{NO(off)} I _{NC(off)}	V ₊ = 3.3 V, V ₋ = 0 V V _{COM} = 0.3, 3 V, V _{NO} , V _{NC} = 3, 0.3 V	Room Full	-1 -10		1 10	nA
	I _{COM(off)}		Room Full	-1 -10		1 10	
Channel On Leakage Current ^a	I _{COM(on)}	V ₊ = 3.3 V, V ₋ = 0 V V _{NO} , V _{NC} = V _{COM} = 0.3, 3 V	Room Full	-1 -10		1 10	
Digital Control^e							
Input Current	I _{INL} or I _{INH}		Full	-1	0.005	1	μA
Dynamic Characteristics							
Turn-On Time	t _{ON}	R _L = 300 Ω, C _L = 35 pF V _{NO} , V _{NC} = 1.5 V See Figure 2	Room Full		140	163 193	ns
Turn-Off Time	t _{OFF}		Room Full		65	80 89	
Break-Before-Make Time Delay	t _D	DG9426 Only, V _{NO} , V _{NC} = 1.5 V R _L = 300 Ω, C _L = 35 pF	Room	5			
Charge Injection ^e	Q _{INJ}	V _g = 0 V, R _g = 0 Ω, C _L = 1 nF	Room		15		pC
Off Isolation ^e	OIRR	R _L = 50 Ω, C _L = 5 pF, f = 1 MHz	Room		-56		dB
Channel-to-Channel Crosstalk ^e	X _{TALK}		Room		-80		
Source Off Capacitance ^e	C _{NO(off)} C _{NC(off)}	f = 1 MHz	Room		53		pF
Drain Off Capacitance ^e	C _{COM(off)}		Room		42		
Channel On Capacitance ^e	C _{COM(on)}		Room		92		

Notes:

- a. Leakage parameters are guaranteed by worst case test conditions and not subject to production test.
- b. Room = 25°C, Full = as determined by the operating temperature suffix.
- c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- e. Guaranteed by design, not subject to production test.
- f. V_{IN} = input voltage to perform proper function.



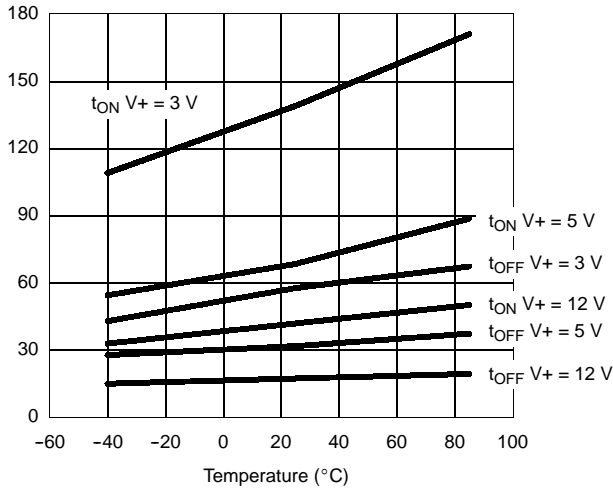
TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



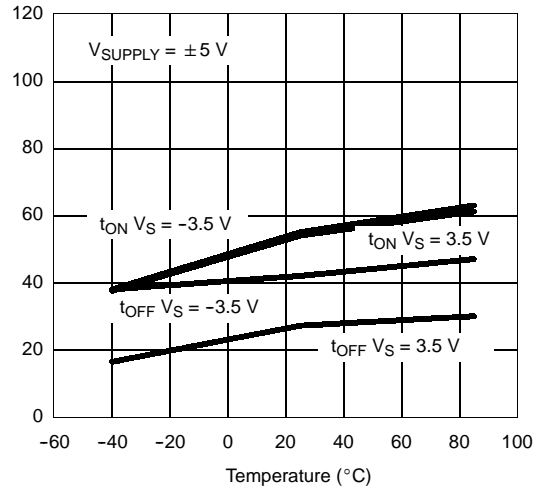


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

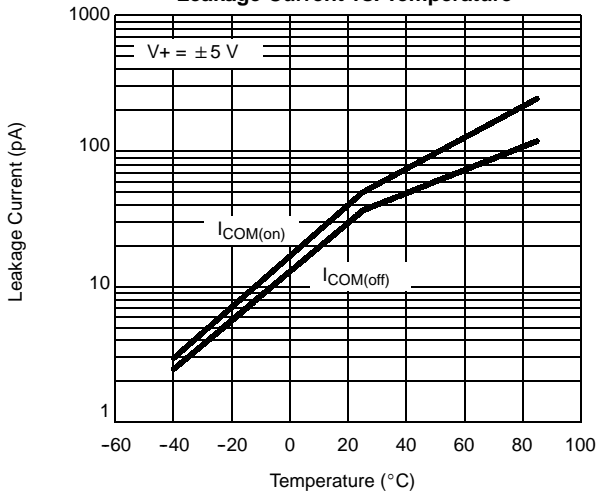
Switching Time vs. Temperature and Single Supply Voltage



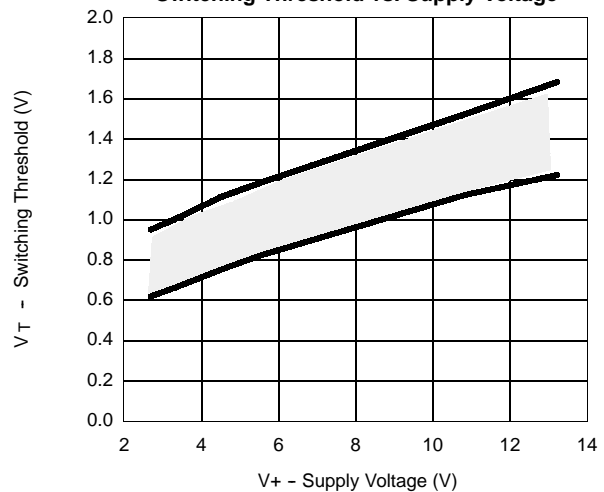
Switching Time vs. Temperature and Dual Supply Voltage



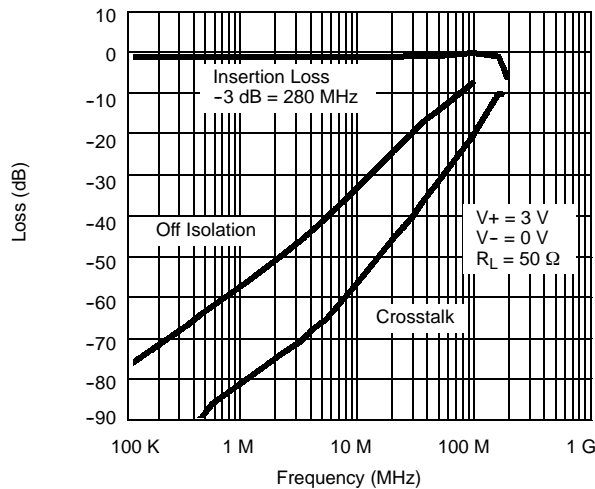
Leakage Current vs. Temperature



Switching Threshold vs. Supply Voltage



Insertion Loss, Off Isolation and Crosstalk vs. Frequency



SCHEMATIC DIAGRAM (TYPICAL CHANNEL)

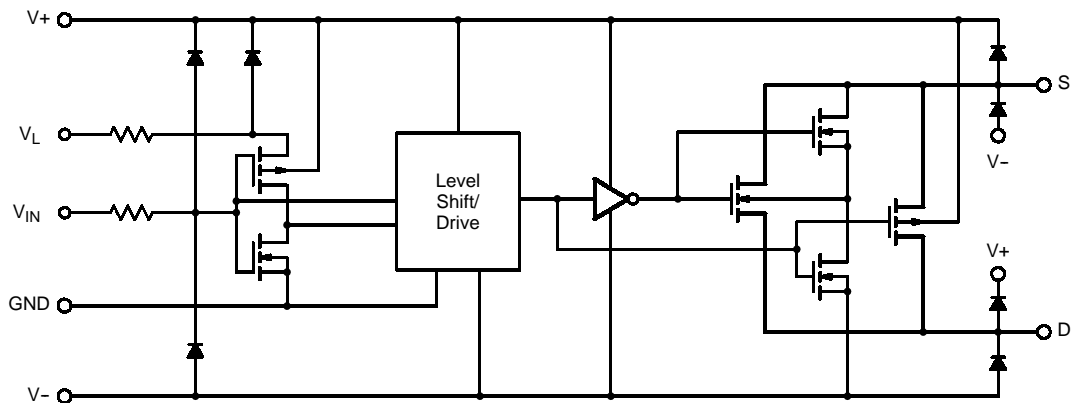
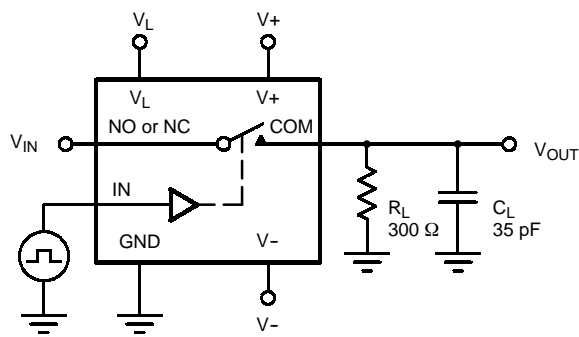


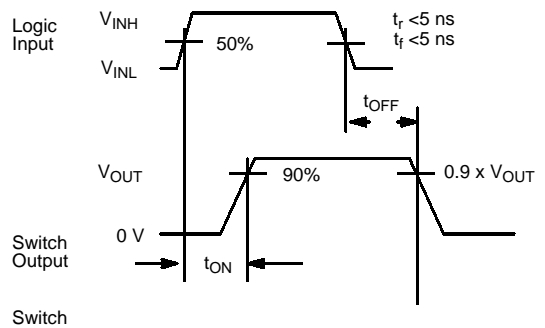
FIGURE 1.

TEST CIRCUITS



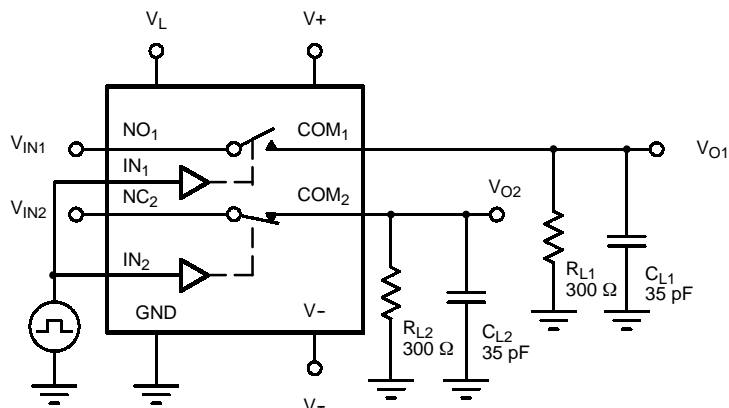
C_L (includes fixture and stray capacitance)

$$V_{OUT} = V_{IN} \frac{R_L}{R_L + r_{ON}}$$



Note: Logic input waveform is inverted for switches that have the opposite logic sense control

FIGURE 2. Switching Time



C_L (includes fixture and stray capacitance)

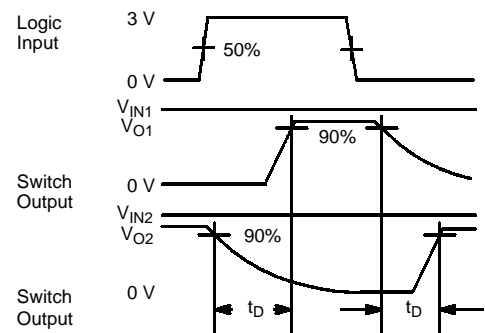
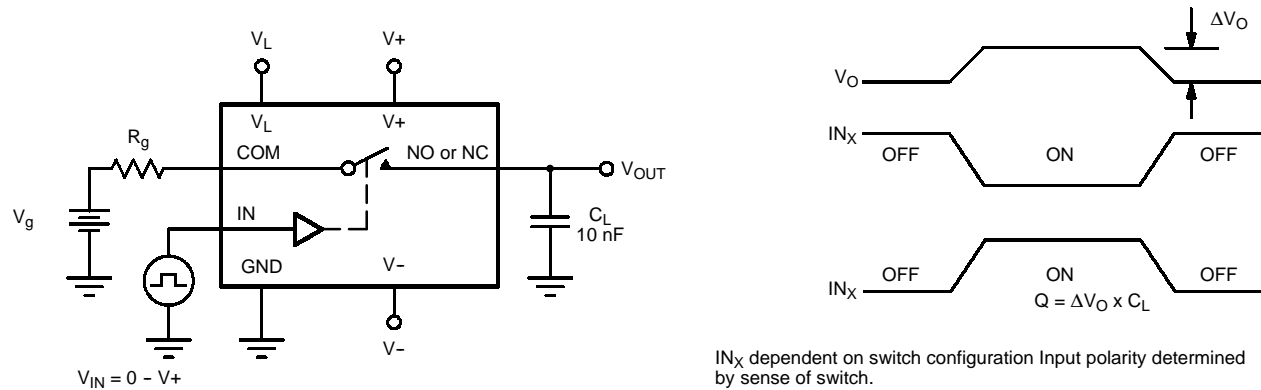
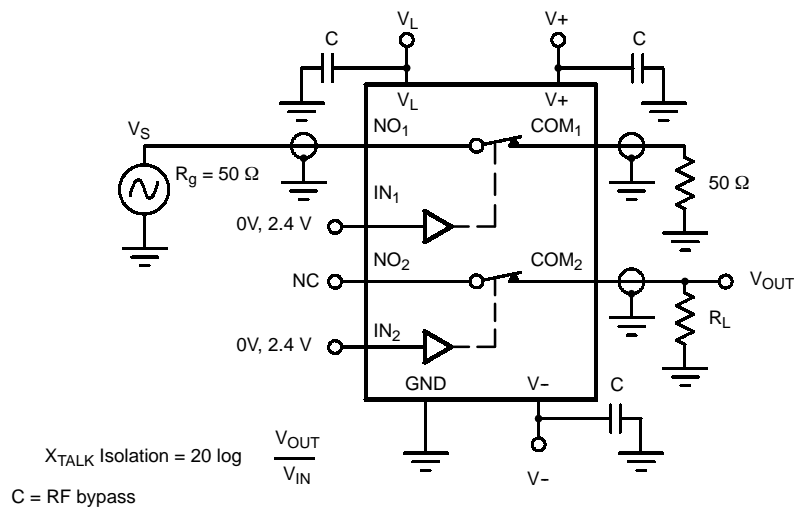
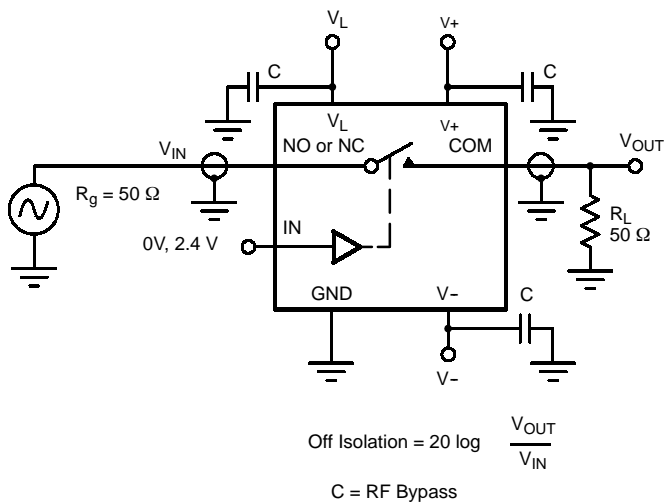
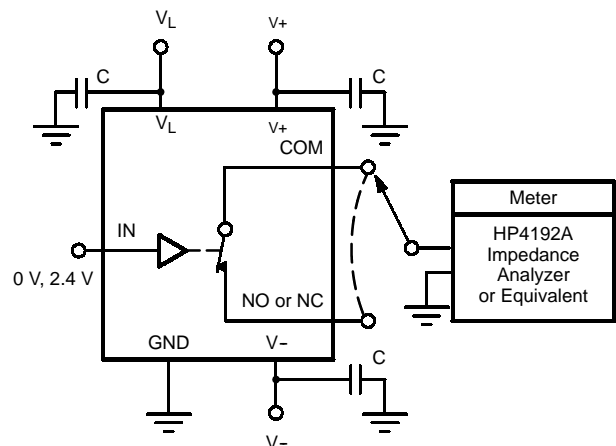


FIGURE 3. Break-Before-Make (DG9426)

TEST CIRCUITS

FIGURE 4. Charge Injection

FIGURE 5. Crosstalk

FIGURE 6. Off Isolation

FIGURE 7. Source/Drain Capacitances



Notice

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